AF 2815

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	28

Application Number	10/689,298
Filing Date	10/20/2003
First Named Inventor	Hsiao
Art Unit	2815
Examiner Name	N. Drew Richards
Attorney Docket Number	184-P065D1C1

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature	Michael P. Adams		
Printed name	Michael P. Adams		
Date	October 14, 2005	Reg. No.	34,763

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Signature	Michael P. Adams		
Typed or printed name	Michael P. Adams	Date	October 14, 2005

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PTO/SB/17 (10-04v2)
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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/689,298
Filing Date	10/20/2003
First Named Inventor	Hsiao
Examiner Name	N. Drew Richards
Art Unit	2815
Attorney Docket No.	184-P065D1C1

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 01-0365

Deposit Account Name: Advanced Micro Devices

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=	
Independent Claims		- 3** =		X	=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	500.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 500.00

SUBMITTED BY

(Complete *(if applicable)*)

Name (Print/Type)	Michael P. Adams	*Registration No. (Attorney/Agent)*	34,763	*Telephone*	512.370.2858
Signature	Michael Adams			*Date*	October 14, 2005

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Hsiao et al.
Serial No.:	10/689,298
Filed:	October 20, 2003
Group Art Unit:	2815
Before the Examiner:	N. Drew Richards
Title:	METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING

APPEAL BRIEF

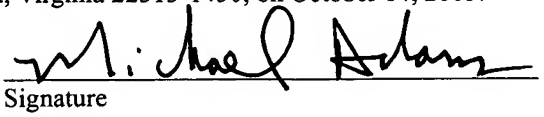
Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 14, 2005.



Signature

Michael P. Adams
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 3-9, and 17-28 are pending in the Application. Claims 1, 3-9, and 17-26 stand rejected. Claims 27 and 28 are withdrawn from consideration. Claims 1, 3-9, and 17-26 are appealed.

IV. STATUS OF AMENDMENTS

Appellants have not submitted any amendments following receipt of the final rejection with a mailing date of June 14, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a method for providing a semiconductor memory device, comprising a plurality of gate stacks having a first and second edge, may comprise the step of providing a source implant adjacent to the first edge of each of the plurality of gate stacks. *See* Specification, page 10, lines 4-12; Specification, page 11, line 23 to page 12, line 4; Claim 1, lines 1-7 (steps a-b); Claim 19, lines 1-4; Figure 3, steps 102, 104; Figure 4, steps 152, 154. The method may further comprise a source implant step that includes a DDI implant and optionally, a second MDDI implant, performed only for the source. *See* Specification, page 10, lines 4-12; Specification, page 11, line 23 to page 12, line 4; Figure 3, step 104; Figure 4, step 154; Claim 3 (step b1); Claims 20-21. The method may further comprise the step of driving the source implant under the first edge of the plurality of gate stacks. This driving step may be accomplished by

annealing the source implant. *See* Specification, page 10, lines 13-21; Specification, page 11, lines 5-12; Figure 3, step 106; Figure 4, step 156; Claim 1 (step c);Claim 3 (step c1); Claims 17-18 and 22-23; Claim 19, lines 5-6. The method may further comprise the step of providing a drain implant, after driving the source implant, adjacent to the second edge of each of the plurality of gate stacks. *See* Specification, page 10, line 22 to page 11, line 3; Specification, page 12, lines 13-17; Figure 3, step 108; Figure 4, step 158; Claim 1 (step d); Claim 7; Claim 19, lines 7-8. The method may further comprise the step of driving the drain implant under the second edge of the plurality of gate stacks. This driving step may be accomplished by thermal cycling that includes a rapid thermal anneal of the drain implant. *See* Specification, page 11, lines 3-9; Specification, page 12, lines 18-23; Figure 3, step 110; Figure 4, step 160; Claim 9; Claims 24-25. In another embodiment, the method may further comprise providing a first spacers on one side of the gate stack and a second spacer on the opposite side of the gate stack. The method may generally include depositing insulating layers and etching the layers to form the spacers. *See* Specification, page 12, line 23 to page 13, line 9; Figure 4, step 162; Claims 4, 6, and 26. The method may further comprise the step of performing a self-aligned source etch of field isolation regions between sources. *See* Specification, page 13, lines 11-12; Figure 4, step 164; Claim 5.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 3-5, 7-8, 17, and 19-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Chen et al.* (U.S. Patent No. 5,482,881) (hereinafter *Chen*). Claims 9, 24, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Gardner et al.* (U.S. Patent No. 5,953,613) (hereinafter *Gardner*). Claims 6 and 26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Miyata et al.* (U.S. Patent No. 5,183,773)

(hereinafter *Miyata*). Claims 22 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Shah et al.* (U.S. Patent No. 5,065,208) (hereinafter *Shah*).

Furthermore, claims 1, 3, 4, 6-9, 17-19, and 24-26 are rejected under the judically created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,235,584, *Sun et al.* (hereinafter "the *Sun* patent"). Claims 5, 20, and 21 are rejected under the judically created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of the *Sun* patent in view of *Chen*. Claims 22 and 23 are rejected under the judically created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of the *Sun* patent in view of *Shah*.

VII. ARGUMENT

A. Claims 1, 3-5, 7-8, 17, and 19-21 are not properly rejected under 35 U.S.C. §102(b).

The Examiner has rejected claims 1, 3-5, 7-8, 17, and 19-21 under 35 U.S.C. §102(b) as being anticipated by *Chen*. *See* Office Action from 06/14/2005, p. 2, lines 9-10. Appellants respectfully traverse these rejections for at least the reasons stated below. Appellants note that the numbering of elements in *Chen*, particularly in Fig. 6 and Figs. 6A-6D, is not unique and consistent among Figures and also is not consistent between the Figures and the Specification. Appellants have provided the numbering as it appears in the Figures of *Chen*.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

1. Claim 1 is not anticipated by *Chen.*

Regarding claim 1, the Examiner states that: **"Chen discloses in figures 3, 6, 6e, and 6f providing a drain implant (672, MDD2, 114,) after, the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks."** *See* Office Action from 06/14/2005, p. 2, lines 19-22. Appellants respectfully traverse. Contrary to the Examiner's assertion, Appellants respectfully assert that *Chen* does not disclose "providing a drain implant after step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks," as recited in claim 1 (emphasis added). Appellants respectfully assert that *Chen* instead discloses :

> Following the intermediate n+ implant MDD1, a second n+ implant MDD2 is suitably provided (step 672) to implant a second predetermined dose of n+ dopants (FIG. 6E). In general, the second predetermined dose of dopant provided by MDD2 is in the range of 1.times.10.sup.14 /cm.sup.2 to 15.times.10.sup.15 /cm.sup.2, and preferably, in the range of 5.times.10.sup.14 /cm.sup.2 to 10.times.10.sup.15 /cm.sup.2, and most preferably, in the range of 2.times.10.sup.15 /cm.sup.2 to 6.times.10.sup.15 /cm.sup.2. The dose provided by MDD2 is suitably the full dose provided by a conventional MDD. Alternatively, the dosage of MDD2 may be reduced by the amount of the intermediate n+ implant MDD1 already performed. Providing intermediate n+ implant MDD1 with a full n+ implant dose MDD2 suitably further enhances the doping concentration in tunneling region 140. *Chen,* col. 8, line 61 to col. 9, line 7.

Chen discloses a second MDD2 implant that is clearly performed simultaneously on the source and the drain. *Chen,* Fig. 6E. In *Chen*, Fig. 6E, there is clearly no mask applied, as in *Chen,* Figs. 6A-6C. Furthermore, *Chen* clearly teaches that the motivation for this step comprises enhancing the doping concentration in the tunneling region 140, which refers to tunneling across dielectric 120, between floating gate 122 and source 112. *Chen,* col. 7, lines 17-21; Fig. 1. There is no language in *Chen* referring to a "drain implant", and *Chen* does not teach the concept of a "drain implant" being performed separately from the source implant, as in claim 1. Each mention of "source implant" and "drain implant" in embodiments of the present invention is mutually exclusive. *See* Fig. 3, steps 104, 108; Fig. 4, steps 154,

158. In the description of the source implant, the term MDDI (moderately doped drain implant) is clearly designated as being "only performed for the source." *See* Specification, page 10, lines 7-8. The Application clearly teaches a distinctive source implant, and therefore, a distinctive drain implant. There is no mention in the Application of the drain implant being performed on the source and the drain. In Appellants' application, a "drain implant" exclusively refers to an implant being applied solely to the drain. Thus, the rejection of claim 1 over *Chen* relies upon the Examiner's interpretation of a "drain implant" that is not supported by the specification. Accordingly, *Chen* does not disclose all of the limitations of claim 1 and does not anticipate it. M.P.E.P. §2131.

2. Claim 3 is not anticipated by *Chen.*

Claim 3 depends from claim 1 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(1) of this paper.

3. Claim 4 is not anticipated by *Chen.*

Claim 4 depends from claim 1 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(1) of this paper.

Contrary to the Examiner's statement, *see* Office Action from 06/14/2005, p. 3, lines 5-9, *Chen* does not disclose the method of claim 1, further comprising the step of "providing a first spacer and a second spacer for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks" as in clam 4. The Examiner cites Figs. 3, 6, 6B-6D, and 6F and insulating layer 720 of *Chen* as disclosing the abovementioned claim limitation. Appellants respectfully traverse. Appellants respectfully assert that insulating layer 720 in *Chen* is clearly described as an oxidation sealing layer that is grown over the

entire array of gate stacks. *Chen*, col. 9, lines 7-8; Fig. 6, step 466; Fig. 6F. There is no mention in *Chen* of spacers disposed along the edge of a plurality of gate stacks as in claim 4. Accordingly, *Chen* does not disclose all of the limitations of claim 4 and does not anticipate it. M.P.E.P. §2131.

4. Claim 5 is not anticipated by *Chen.*

Claim 5 depends from claim 4 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(2) of this paper.

Contrary to the Examiner's statement, *see* Office Action from 06/14/2005, p. 3, lines 10-11, Chen does not disclose the method of claim 4, further comprising the step of "providing a self-aligned source etch" as in clam 5. The Examiner cites element 454 of *Chen* as disclosing the abovementioned claim limitation. Appellants respectfully traverse. The etch in *Chen* is clearly described as a selective etch performed after masking the drain regions, but before any implant steps have been performed. *Chen,* col. 8, lines 25-32; Fig. 6, 452, 454. There is no mention in Chen of performing the etch as a subsequent step, as in claim 5. Accordingly, *Chen* does not disclose all of the limitations of claim 5 and does not anticipate it. M.P.E.P. §2131.

5. Claims 7 is not anticipated by *Chen.*

Claim 7 depends from claim 1 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(1) of this paper.

6. Claim 8 is not anticipated by *Chen.*

Claim 8 depends from claim 3 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(2) of this paper.[1]

7. Claim 17 is not anticipated by *Chen.*

Claim 17 depends from claim 1 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(1) of this paper.

8. Claim 19 is not anticipated by *Chen.*

Regarding claim 19, the Examiner states that: **"Chen discloses in figures 3 and 6-6f, after the source implant diffuses under the first edge of the stacked gate, performing a drain implant adjacent to a second edge of the stacked gate."** *See* Office Action from 06/14/2005, p. 4, lines 5-7. Appellants respectfully traverse. Contrary to the Examiner's assertion, Appellants respectfully assert that *Chen* does not disclose "performing a drain implant" as recited in claim 19. Appellants respectfully assert that *Chen* instead discloses a second MDD2 implant that is clearly performed simultaneously on the source and the drain. *Chen,* Fig. 6E. In *Chen,* Fig. 6E, there is clearly no mask applied, as in *Chen,* Figs. 6A-6C. Furthermore, *Chen* clearly teaches that the motivation for this step comprises enhancing the doping concentration in the tunneling region 140, which clearly refers to tunneling across dielectric 120, between floating gate 122 and source 112. *Chen*, col. 7, lines 17-21, *Fig. 1.* There is no language in *Chen* referring to a "drain implant", and *Chen* does not teach the concept of a "drain implant", whereby the drain implant is performed separately from the source implant, as in claim 19. Each mention of "source implant" and "drain implant" in embodiments of the present invention is mutually exclusive.

[1] Claim 8 erroneously states that it depends on claim 5, instead of claim 3. Upon allowance, Appellants will amend this claim accordingly.

See Fig. 3, steps 104, 108; Fig. 4, steps 154, 158. In the description of the source implant, the term MDDI (moderately doped drain implant) is clearly designated as being "only performed for the source." *See* Specification, page 10, lines 7-8. The Application clearly teaches a distinctive source implant, and therefore, a distinctive drain implant. There is no mention in the Application of the drain implant being performed on the source and the drain. In Appellants' application, a "drain implant" exclusively refers to an implant being applied solely to the drain. Thus, the rejection of claim 19 over *Chen* relies upon the Examiner's interpretation of a "drain implant" that is not supported by the specification. Accordingly, *Chen* does not disclose all of the limitations of claim 19 and does not anticipate it. M.P.E.P. §2131.

9. Claim 20 is not anticipated by *Chen.*

Claim 20 depends from claim 19 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(8) of this paper.

10. Claim 21 is not anticipated by *Chen.*

Claim 21 depends from claim 19 and hence is not anticipated by *Chen* for at least the reasons presented above in Section (A)(8) of this paper.

B. Claims 9, 24 and 25 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Gardner*.

The Examiner has rejected claims 6 and 26 under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Gardner*. *See* Office Action from 06/14/2005, p. 5, lines 1-3. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not provided a source of motivation for combining *Chen* with *Gardner*

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner has not presented a source for his motivation for modifying *Chen* with *Gardner*. The motivation to modify *Chen* with *Gardner* must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided sufficient evidence that his motivation to combine for achieving Appellants' claimed invention comes from any of these sources. In particular, *Gardner* clearly teaches away from the present invention.

> In accordance with an aspect of the present invention, the removal or detachment of an electron source from the semiconductor substrate eliminates the heavily-doped source drain diffusion or implant into a source region of the substrate, thereby avoiding non-uniform doping profiles that degrade short-channel subthreshold characteristics of a device as well as the punchthrough behavior of short-channel devices. *Gardner*, col. 2, lines 8-15, emphasis added.
>
> In accordance with an aspect of some embodiments of the present invention, a conventional LDD process flow for forming a MOSFET on a substrate is minimally modified, first by only implanting a drain region and not the source during a source drain implant,... *Gardner*, col. 2, lines 21-25, emphasis added.
>
> Following implanting of the P-channel drain region 122 and the N-channel drain region 124, the P-channel transistor 106 has a P-channel source region 126 that is not doped. The N-channel transistor 110 has an N-channel source region 128 that is not doped. Thus, the illustrative semiconductor structure, in contrast to conventional LDD structures, has no implant dopant in source regions except for LDD doping. *Gardner*, col. 7, lines 61-67, emphasis added.

Gardner therefore does not provide motivation to combine with *Chen*, since *Gardner* teaches away from implanting the source region of the substrate, whereby the present invention teaches providing a drain implant after driving the source implant. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 9, 24, and 25. *Id.*

2. The Examiner is using improper hindsight reasoning in combining *Chen* with *Gardner*.

Furthermore, the Examiner's conclusion of obviousness is based on improper hindsight reasoning. The Examiner's motivations appear to have been gleaned from Appellants' disclosure. The Examiner states that:

> **It would have been further obvious to one of ordinary skill in the art at the time that of the present invention to use the rapid thermal annealing step of Gardner in the method of Chen and Gardner in order**

to activate the drain dopants and remove crystalling damage as taught by Gardner in column 7, lines 49-52. *See* Office Action from 06/14/2005, p. 5, lines 8-12.

Appellants respectfully traverse. *Chen* does not teach a drain implant, as in Appellants' invention. Therefore, only Appellants' invention provides motivation to introduce a drain implant in *Chen* and then provide a rapid thermal anneal for that drain implant. Any judgment on obviousness must not include knowledge gleaned from Appellants' disclosure. *In re McLaughlin*, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 9, 24, and 25. M.P.E.P. §2145.

3. The combination of *Chen* with *Gardner* is not enabling.

Appellants also respectfully assert that the method of making non-volatile flash EEPROM memory of *Chen* is not compatible with the process for forming the high performance MOSFET of *Gardner*, particularly since *Gardner* teaches away from a source implant and "eliminates the heavily-doped source drain diffusion or implant into a source region of the substrate...." *Gardner*, Abstract, lines 6-8. The combination of *Chen* with *Gardner* appears to create an inoperable reference that under the case law may be considered to teach away from the combination. *In re Gordon*, 221 USPQ 1125, 1127 (C.A.F.C. 1984).

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 9, 24, and 25. M.P.E.P. §2143.

C. Claims 6 and 26 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Miyata*.

The Examiner has rejected claims 6 and 26 under 35 U.S.C. §103(a) as being

unpatentable over *Chen* in view of *Miyata*. *See* Office Action from 06/14/2005, p. 6, lines 4-6. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not provided a source of motivation for combining *Chen* with *Miyata*.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner has not presented a source for his motivation for modifying *Chen* with *Miyata*. The motivation to modify *Chen* with *Miyata* must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided sufficient evidence that his motivation to combine for achieving Appellants' claimed invention comes from any of these sources. In particular, there is no language in *Miyata* that mentions providing a drain implant after a source implant has been driven. Furthermore, *Miyata* clearly mentions an EPROM memory device that requires UV radiation for erasure: "When electrons stored in the floating gate 78 are discharged from the memory cell, ultraviolet rays are directed to the cell." *Miyata*, col. 5, lines 16-18. Therefore, *Miyata* does not disclose a memory device that suffers

from short channel effects as pertains to Appellants' invention, and *Miyata* does not mention driving a drain or source implant under the edge of a gate stack. Since *Miyata* cannot be considered analogous art with *Chen* or with Appellants' invention, there is no motivation to combine *Chen* with *Miyata*. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 6 and 26. *Id.*

2. The Examiner is using improper hindsight reasoning in combining *Chen* with *Miyata*.

Furthermore, the Examiner's conclusion of obviousness is based on improper hindsight reasoning. The Examiner's motivations appear to have been gleaned from Appellants' disclosure. The Examiner states that:

> **It would have been obvious to one of ordinary skill in the art at the time that of the present invention to use the peripheral logic devices and concurrent spacer forming step of Miyata in the method of Chen in order to save space on a mother board and therefore reduce costs of fabrication by further consolidating fabrication steps.** *See* Office Action from 06/14/2005, p. 6, lines 16-20.

Appellants respectfully traverse. It is Appellants' disclosure that provides the inventive aspect of consolidating fabrication steps, not *Chen* or *Miyata*. Any judgment on obviousness must not include knowledge gleaned from Appellants' disclosure. *In re McLaughlin*, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 3, 16 and 42. M.P.E.P. §2145.

As a result of the foregoing, Applicant respectfully asserts that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 6 and 26. M.P.E.P. §2143.

D. Claims 22 and 23 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Shah*.

The Examiner has rejected claims 22 and 23 under 35 U.S.C. §103(a) as being unpatentable over *Chen* in view of *Shah*. *See* Office Action from 06/14/2005, p. 7, lines 1-3. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not provided a source of motivation for combining *Chen* with *Shah*.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner has not presented a source for his motivation for modifying *Chen* with *Shah*. The motivation to modify *Chen* with *Shah* must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149

F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided sufficient evidence that his motivation to combine for achieving Appellants' claimed invention comes from any of these sources. *Shah* does not mention any kind of semiconductor memory, as in claims 22 and 23. In particular, there is no language in *Shah* that mentions providing a drain implant after a source implant has been driven in a semiconductor memory. Since *Shah* cannot be considered analogous art with the present invention, there is no motivation to combine *Chen* with *Shah*. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 22 and 23. *Id.*

2. The Examiner is using improper hindsight reasoning in combining *Chen* with *Shah*.

Furthermore, the Examiner's conclusion of obviousness is based on improper hindsight reasoning. The Examiner's motivations appear to have been gleaned from Appellants' disclosure. The Examiner states that:

> **Shah teaches in column 10, lines 33-37 wherein heat treating a semiconductor memory comprises annealing the semiconductor memory in a furnace at about 900 degrees Celsius for about 40 minutes. It would have been obvious to one of ordinary skill in the art at the time that of the present invention to use the annealing of Shah in the method of Chen in order to drive an N type impurity of a source region under gate oxide as taught by Shah in column 10, lines 33-37.** *See* Office Action from 06/14/2005, p. 7, lines 7-12.

Appellants respectfully traverse. *Shah* does not teach annealing a semiconductor memory. *Shah* instead teaches concurrent annealing of both the source and the drain

of a logic transistor. The motivation to anneal a semiconductor memory source implant arises from Appellants' invention, not *Chen* or *Shah*. Any judgment on obviousness must not include knowledge gleaned from Appellants' disclosure. *In re McLaughlin*, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 22 and 23. M.P.E.P. §2145.

3. The combination of *Chen* with *Shah* is not enabling.

Appellants also respectfully assert that the method of making non-volatile flash EEPROM memory of *Chen* is not compatible with the process for fabricating bipolar and CMOS transistors of *Shah*. *Shah* does not teach annealing a semiconductor memory. Further, *Shah* teaches annealing both the source and the drain of a logic transistor simultaneously. *Shah*, col. 10, lines 33-37. The combination of *Chen* with *Shah* creates an inoperable reference that under the case law may be considered to teach away from the combination. *In re Gordon*, 221 USPQ 1125, 1127 (C.A.F.C. 1984).

As a result of the foregoing, Applicant respectfully asserts that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 22 and 23. M.P.E.P. §2143.

E. Statement regarding Terminal Disclaimer for double patenting rejection of claims 1, 3-9, and 17-26.

Upon allowance of claims 1, 3-9, and 17-26, Appellants will submit an appropriate Terminal Disclaimer and fees to overcome the Examiner's obviousness-type double patenting rejection over the *Sun* patent.

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1, 3-9, and 17-26 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1, 3-9, and 17-26.

Respectfully submitted,
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CLAIMS APPENDIX

1. A method for providing a semiconductor memory device including a substrate and at least one field isolation region, the method comprising the steps of:

(a) providing a plurality of gate stacks above the substrate, each of the plurality of gate stacks including a first edge and a second edge, each of the plurality of gate stacks crossing the at least one field isolation region;

(b) providing a source implant adjacent to the first edge of each of the plurality of gate stacks;

(c) driving the source implant under the first edge of each of the plurality of gate stacks; and

(d) providing a drain implant after step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks.

3. The method of claim 1 wherein the source implant providing step (b) includes the step of:

(b1) providing a first source implant and a second source implant adjacent to the first edge of each of the plurality of gate stacks; and

wherein the driving step (c) includes the step of:

(c1) driving the first source implant and the second source implant under the first edge of each of the plurality of gate stacks.

4. The method of claim 1 further comprising the step of:

(e) providing a first spacer and a second spacer for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks.

5. The method of claim 4 further comprising the step of:

(f) providing a self-aligned source etch.

6. The method of claim 4 wherein the semiconductor memory device further includes a periphery including a plurality of logic devices and wherein the spacer providing step (e) further includes the step of:

(e1) providing the first spacer and the second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device.

7. The method of claim 1 wherein the drain implant is As.

8. The method of claim 5 wherein the second source implant is As.

9. The method of claim 1 further comprising the step of:

(e) providing a rapid thermal anneal after the drain implant has been provided.

17. The method of claim 1 wherein the step of driving the source implant under the first edge of each of the plurality of gate stacks comprises a thermal treatment.

18. The method of claim 3 wherein the step of driving the first and second source implants under the first edge of each of the plurality of gate stacks comprises a thermal treatment.

19. A method of fabricating a semiconductor memory, the method comprising:

forming a stacked gate;

performing a source implant adjacent to a first edge of the stacked gate;

heat treating the semiconductor memory so that the source implant diffuses under the first edge of the stacked gate;

after the source implant diffuses under the first edge of the stacked gate, performing a drain implant adjacent to a second edge of the stacked gate; and

wherein the source implant extends further under the first edge of the stacked gate than the drain implant extends under the second edge of the stacked gate.

20. The method of claim 19 wherein performing the source implant comprises performing a double diffused implant (DDI).

21. The method of claim 19 wherein performing the source implant comprises:

performing a double diffuse implant (DDI); and

performing a moderately doped drain implant (MDDI).

22. The method of claim 19 wherein heat treating the semiconductor memory comprises annealing the semiconductor memory at a temperature of between about 800° and about 1000° Celsius for about 20 to about 200 minutes.

23. The method of claim 22 wherein annealing the semiconductor memory comprises heating the semiconductor memory in a furnace at about 900° Celsius for about 40 minutes.

24. The method of claim 19 further comprising performing a rapid thermal anneal after performing the drain implant.

25. The method of claim 24 wherein the rapid thermal anneal comprises heat treating the semiconductor memory in a furnace at a temperature of about 900° to about 1000° Celsius for about 10 to about 30 seconds.

26. The method of claim 19 further comprising forming first and second spacers adjacent the first and second edges, respectively.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.